

AZ DISPLAYS, INC.

COMPLETE LCD SOLUTIONS

SPECIFICATIONS FOR LIQUID CRYSTAL DISPLAY

PART NUMBER: □□ □ □ ACM1602Z SERIES

DATE: □ □ □ □ □ □ APRIL 12, 2007

1.0 MECHANICAL SPECS

1. Overall Module Size (W*H*T)	41.2*47.5 *2.1(MAX)mm
2. Viewing Area (W*H)	38.2X17.0mm
3. Dot Size	0.34*0.50
4. Dot Pitch	0.38*0.58
5. Driving Method	1/17D, 1/5B,4.8V
6. Controller IC	ST7032I
7. LCD Type	STN(GRAY) ,Positive ,Reflective
8. Viewing Direction	6 O'Clock
9. Interface	I ² C
10. Backlight	NO
11. Operating Temperature	Wide (-20°C ~ 70°C)
12. Rohs	Conforms

2.0 ABSOLUTE MAXIMUM RATINGS

Item	Sy	mbol	Min	Typ	Max	Unit
Operating temperature		Top	-20	-	70	°C
Storage temperature		Tst	-30	-	80	°C
Input voltage		Vin	Vss		Vdd	V
Supply voltage for logic		Vdd- Vss	2.7	-	3.6	V
Supply voltage for LCD drive		Vdd- Vo	3.0		6.5	V

3.0 ELECTRICAL CHARACTERISTICS

3.1 Electrical Characteristics Of LCM

Item	Sy	mbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage		VDD	Ta=25°C	2.8	3.0	3 .2	V
Power Supply Current		Idd	Vdd=3.0V	-		1.0	mA
Input voltage (high)		Vih	H level	2.2	-	Vdd	V
Input voltage (low)		Vil	L level	0	-	0.6	V
Recommended LC Driving Voltage		Vdd -Vo	-20°C	-		5.5	V
			25°C	4.5	4.8	5.0	
			70°C	4 .0		-	

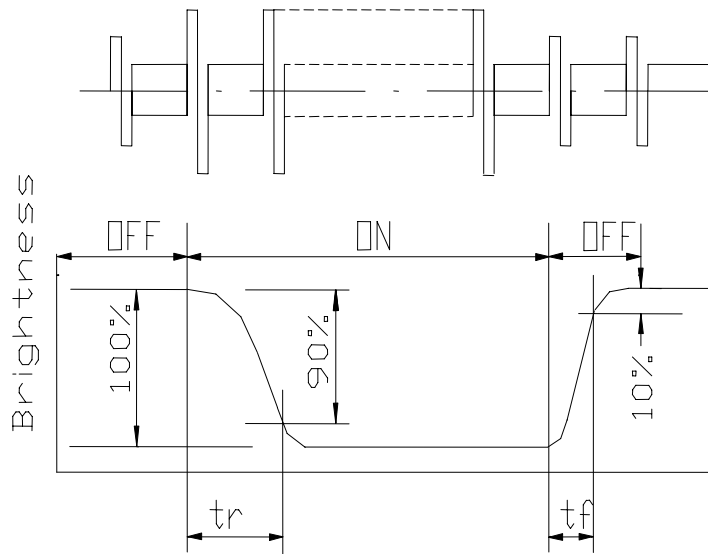
3.2 The Characteristics Of Backlight

Item	Sy	mbol	Condition	Min	Typ	Max	Unit
Operate Current			-		NO		mA

4.0 OPTICAL CHARACTERISTICS (Ta=25°C, Vdd= 5.0V±0.25V, STN LC fluid)

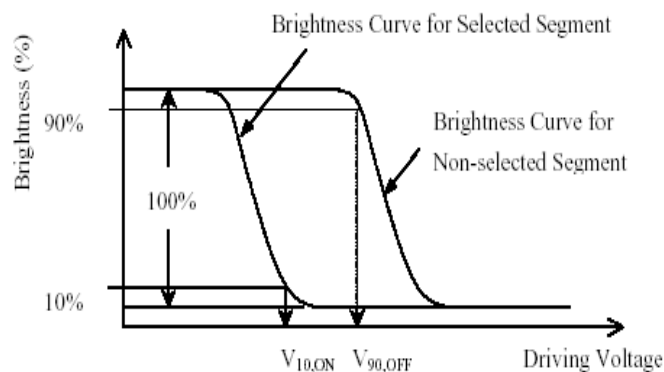
Item	Sy	mbol	Condition	Min	Typ	Max	Unit
Viewing angle (horizontal)	θ	Cr	≥ 2.0	-35	-	35	deg
Viewing angle (vertical)	ϕ	Cr	≥ 2.0	-25	-	45	deg
Contrast Ratio		Cr	$\phi=0^\circ, \theta=0^\circ$	3.0		-	
Response time (rise)		Tr	$\phi=0^\circ, \theta=0^\circ$	-	150	250	ms
Response time (fall)		Tf	$\phi=0^\circ, \theta=0^\circ$	-	160	280	ms

(1). Definition of Optical Response Time

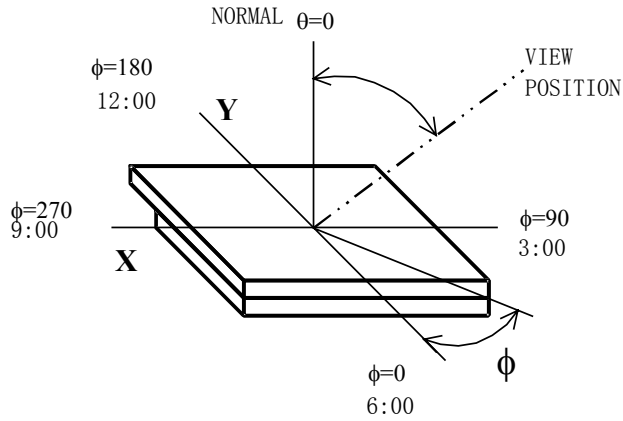


(2). Definition of Driving Voltage (Vlcd)

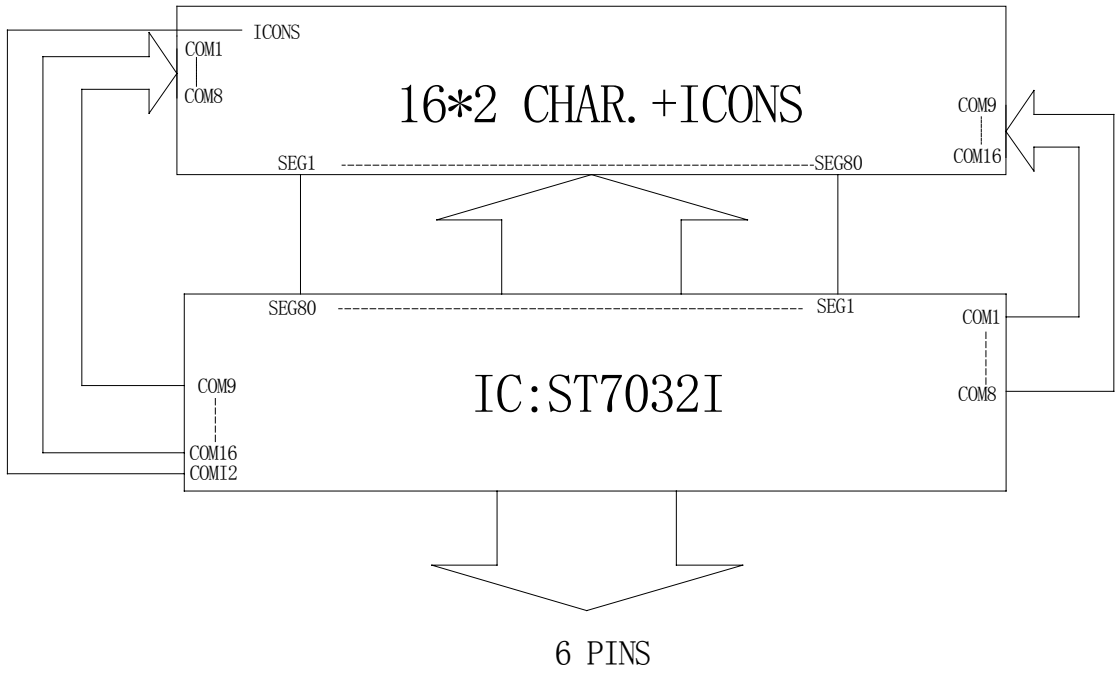
$$V_{lcd} = (V_{10,ON} + V_{90,OFF}) / 2$$



(3). Definition of Viewing Angle and



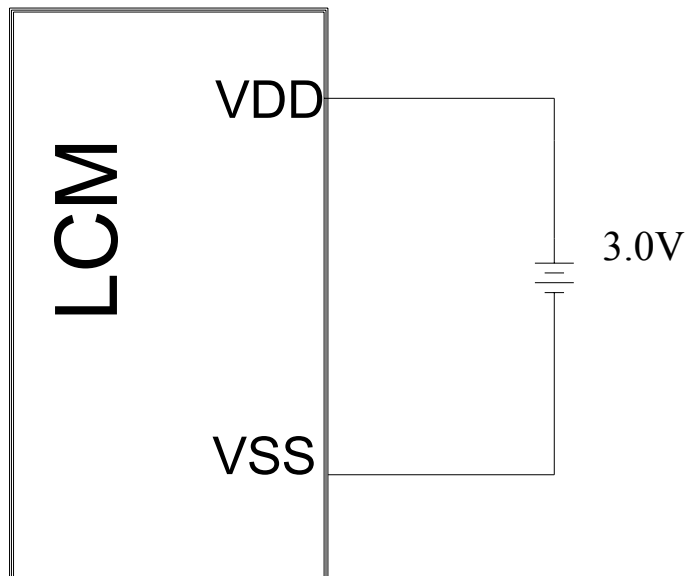
5.0 BLOCK DIAGRAM



6.0 PIN ASSIGNMENT

Pin No.	Symbol	Function
1	VLCD	Power supply for LCD drive
2	VSS	Ground
3	VDD	Power supply
4	SDA	DATA INPUT
5	RST	EXTERNAL RESET PIN
6	SCL	CLOCK INPUT

7.0 POWER SUPPLY

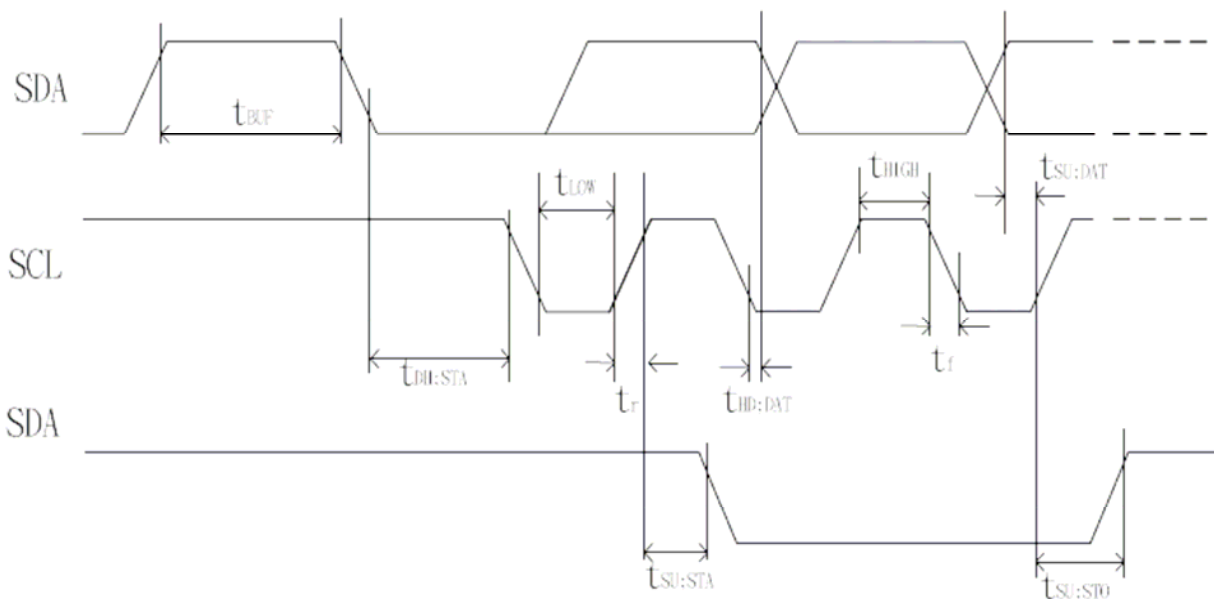


8.0 TIMING CHARACTERISTICS

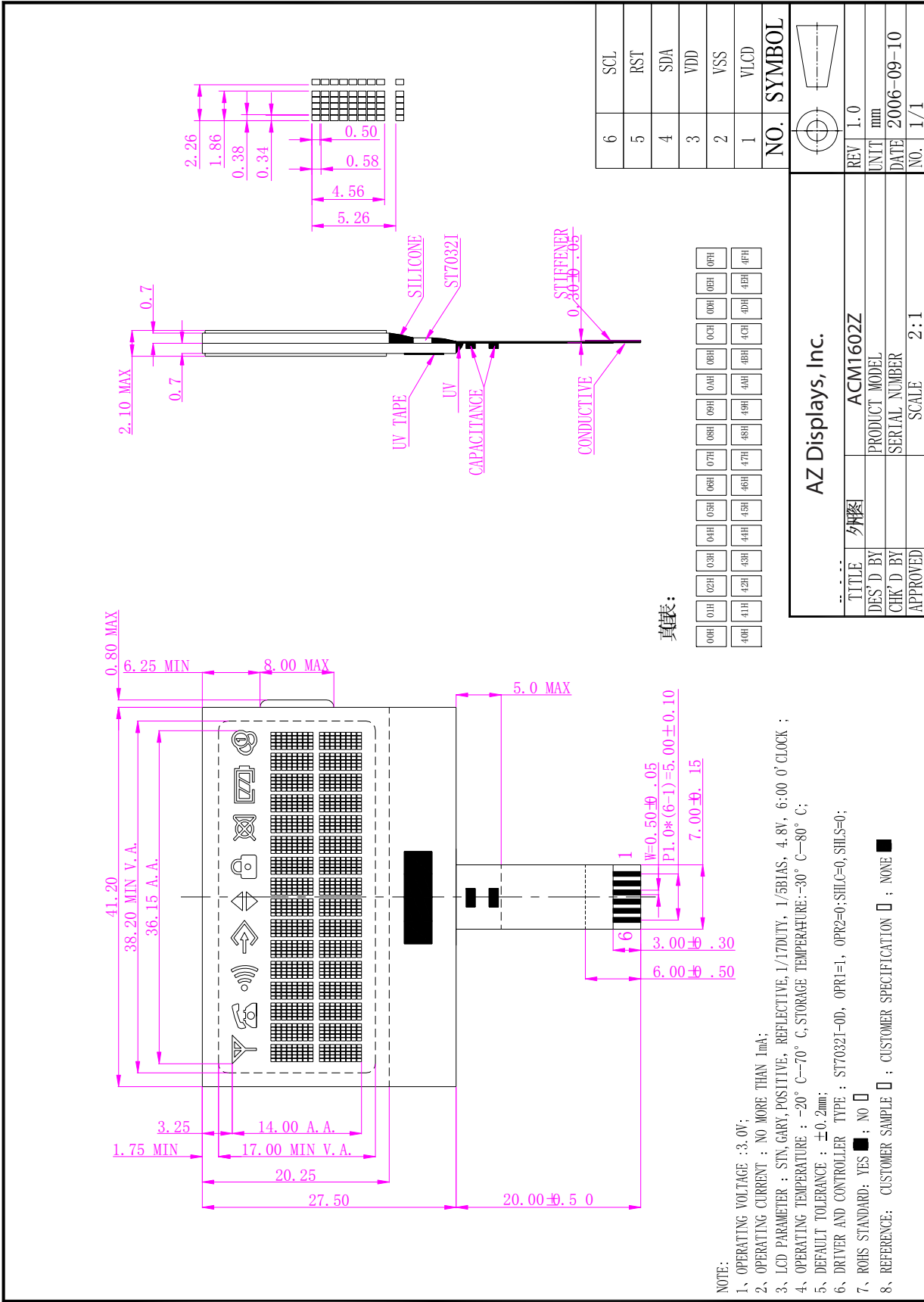
(Ta = -30°C to 85°C)

Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
				SCL clock frequency	SCL	f_{SCLK}	—	
SCL clock low period	t_{LOW}	—	1.3	—		1.3	—	us
SCL clock high period	t_{HIGH}	—	0.6	—		0.6	—	
Data set-up time	SI	$t_{SU:DAT}$	—	180	—	100	—	ns
Data hold time		$t_{HD:DAT}$	—	0	0.9	0	0.9	us
SCL,SDA rise time	SCL, SDA	t_r	—	$20+0.1C_b$	300	$20+0.1C_b$	300	ns
SCL,SDA fall time		t_f	—	$20+0.1C_b$	300	$20+0.1C_b$	300	
Capacitive load represent by each bus line		C_b	—	—	400	—	400	pf
Setup time for a repeated START condition	SI	$t_{SU:STA}$	—	0.6	—	0.6	—	us
Start condition hold time		$t_{HD:STA}$	—	0.6	—	0.6	—	us
Setup time for STOP condition		$t_{SU:STO}$	—	0.6	—	0.6	—	us
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	—	1.3	—	us

I2C interface



9.0 MECHANICAL DIAGRAM



11.0 DISPLAY INSTRUCTION TABLE

Instruction	Instruction Code										Description	Instruction Execution Time			
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		OSC=380KHz	OSC=540kHz	OSC=700KHz	
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms	
Return Home	0	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 us	18.5 us	14.3 us
Display ON/OFF	0	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 us	18.5 us	14.3 us
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	x	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 us	18.5 us	14.3 us
Function Set	0	0	0	0	1	DL	N	x	x	x	DL: interface data is 8/4 bits N: number of line is 2/1	26.3 us	18.5 us	14.3 us	
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	26.3 us	18.5 us	14.3 us	
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 us	18.5 us	14.3 us	
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0	
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM)	26.3 us	18.5 us	14.3 us	
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM)	26.3 us	18.5 us	14.3 us	

Note:

Be sure the ST7032 is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7032. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

b7-b4 b3-b0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	ı	ŕ		ø	ø	P	`	P	ç	é		—	ø	ε	á	´
0001	J	†	!	1	A	Q	a	q	Q	æ	æ	ʔ	ʔ	¿	í	¨
0010	ø	ø	"	2	B	R	b	r	é	É	ƒ	ı	ı	×	ó	°
0011	ʔ	¶	#	3	C	S	c	s	À	à	ı	ı	ʔ	ʔ	ú	˘
0100	ı	ŕ	*	4	D	T	d	t	à	à	\	ı	ı	ı	ı	´
0101	↑	Δ	%	5	E	U	e	u	à	à	•	•	•	ı	ı	ı
0110	↓	θ	&	6	F	V	f	v	à	à	ʔ	ʔ	ı	ı	ı	ı
0111	÷	A	'	7	G	W	g	w	ç	ç	ʔ	ʔ	ʔ	ʔ	ı	ı
1000	÷	E	(8	H	X	h	x	é	é	ı	ı	ı	ı	ı	ı
1001	ŕ	π)	9	I	Y	i	y	è	è	ı	ı	ı	ı	ı	ı
1010	ŕ	Σ	*	:	J	Z	j	z	è	è	ı	ı	ı	ı	ı	ı
1011	L	ŕ	+	:	K	ı	k	(ı	ı	ı	ı	ı	ı	ı	ı
1100	ı	ø	,	<	L	*	ı	ı	ı	ı	ı	ı	ı	ı	ı	ı
1101	•	ψ	—	=	M	ı	m)	ı	ı	ı	ı	ı	ı	ı	ı
1110	ø	Ω	•	>	N	^	n	→	À	À	ı	ı	ı	ı	ı	ı
1111	ø	α	/	?	O	_	o	←	À	À	ı	ı	ı	ı	ı	ı