INTRODUCTION

The KS0108B is a LCD driver LSI with 64 channel output for dot matrix liquid crystal graphic display system. This device consists of the display RAM, 64 bit data latch, 64 bit drivers and decoder logics. It has the internal display RAM for storing the display data transferred from a 8 bit micro controller and generates the dot matrix liquid crystal driving signals corresponding to stored data. The KS0108B composed of the liquid crystal display system in combination with the KS0107B (64 common driver).

FEATURES

- Dot matrix LCD segment driver with 64 channel output
- Input and Output signal
  - Input: 8 bit parallel display data
    Control signal from MPU
    Split bias voltage (V1R, V1L, V2R, V2L, V3R, V3L, V4R, V4L)
  - Output: 64 channel waveform for LCD driving.
- Display data is stored in display data RAM from MPU.
- Interface RAM
  - Capacity: 512 bytes (4096 bits)
  - RAM bit data: RAM bit data = 1:ON
    RAM bit data = 0:OFF
- Applicable LCD duty: 1/32~1/64
- LCD driving voltage: 8V~17V(VDD - VEE)
- Power supply voltage: +5V±10%

<table>
<thead>
<tr>
<th>Driver</th>
<th>Controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>KS0107B</td>
<td>Other KS0108B</td>
</tr>
</tbody>
</table>

- High voltage CMOS process.
- 100QFP and bare chip available.
KS0108B  64CH SEGMENT DRIVER FOR DOT MATRIX LCD

Fig. 2. 100QFP Top View
## PIN DESCRIPTION

<table>
<thead>
<tr>
<th>PIN (NO)</th>
<th>SYMBOL</th>
<th>INPUT/OUTPUT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
| 3, 78, 73, 8 | VDD, VSS, VEE1.2 | Power | For internal logic circuit (+5V±10%)
| | | | GND (0V)
| | | | For LCD driver circuit
| | | | VDD=5V, VSS=0V, VEE=18V-17V
| | | | VEE1 and VEE2 is connected by the same voltage. |
| 74, 76, 77, 75, 6 | V0L, V0R, V2L, V2R, V3L, V3R | Power | Bias supply voltage terminals to drive the LCD. |
| 92, 91, 90 | CS1B, CS2B, CS3 | Input | Chip selection
| | | | In order to interface data for input or output
| | | | The terminals have to be CS1B=L, CS2B=L, and CS3=H. |
| 2 | M | Input | Alternating signal input for LCD driving. |
| 1 | ADC | Input | Address control signal of Y address counter.
| | | | ADC=H→DB<0:7>=0→Y0→S1
| | | | DB<0:7>=63→Y63→S64
| | | | ADC=L→DB<0:7>=0→Y63→S64
| | | | DB<0:7>=63→Y0→S1 |
| 100 | FRM | Input | Synchronous control signal.
| | | | Presets the 6-bit Z counter and synchronizes the common signal with the frame signal when the frame signal becomes high. |
| 99 | E | Input | Enable signal.
| | | | write mode (R/W=L) → data of DB<0:7> is latched at the falling edge of E. |
| | | | read mode (R/W=H) → DB<0:7> appears the reading data while E is at high level. |
| 98, 97 | CLK1, CLK2 | Input | 2 phase clock signal for internal operation.
| | | | Used to execute operations for input/output of display RAM data and others. |
| 96 | CL | Input | Display synchronous signal.
| | | | Display data is latched at rising time of the CL signal and increments the Z-address counter at the CL falling time. |
| 95 | RS | Input | Data or Instruction.
| | | | RS=H→DB<0:7> : Display RAM Data
| | | | RS=L→DB<0:7> : Instruction Data |
| 94 | R/W | Input | Read or Write.
| | | | R/W=H → Data appears at DB<0:7> and can be read by the CPU while E=H, CS1B=L, CS2B=L and CS3=H.
| | | | R/W=L→Display data DB<0:7> can be written at falling of E when CS1B=L, CS2B=L and CS3=H. |
| 79~86 | DB0~DB7 | Input/Output | Data bus.
| | | | There state I/O common terminal. |
## PIN DESCRIPTION

### PIN (NO)  NAME  INPUT/OUTPUT  DESCRIPTION

<table>
<thead>
<tr>
<th>PIN (NO)</th>
<th>NAME</th>
<th>INPUT/OUTPUT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>72~9</td>
<td>S1~S64</td>
<td>Output</td>
<td>LCD Segment driver output. Display RAM data 1:ON Display RAM data 0:OFF (Relation of display RAM data &amp; M)</td>
</tr>
<tr>
<td>93</td>
<td>RSTB</td>
<td>Input</td>
<td>Reset signal. When RSTB=L, (1) ON/OFF register becomes set by 0. (display off) (2) Display start line register becomes set by 0 (Z-address 0 set, display from line 0) After releasing reset, this condition can be changed only by instruction.</td>
</tr>
<tr>
<td>87~89</td>
<td>NC</td>
<td>No connection. (open)</td>
<td></td>
</tr>
</tbody>
</table>

### MAXIMUM ABSOLUTE LIMIT

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Voltage</td>
<td>VDD</td>
<td>-0.3~+7.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>VEE</td>
<td>VDD-19.0~VDD+0.3</td>
<td>V</td>
<td>*4</td>
</tr>
<tr>
<td>Driver Supply Voltage</td>
<td>VDD</td>
<td>-0.3~VDD+0.3</td>
<td>V</td>
<td>*1,3</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>VDD</td>
<td>VEE-0.3~VDD+0.3</td>
<td>V</td>
<td>*2</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>TOPR</td>
<td>-30~+85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>TSTB</td>
<td>-55~+125</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

*1. Based on VSS=0V.
*2. Applies the same supply voltage to VEE1 and VEE2. VDD=VDD; VEE=VEE.
*3. Applies to M, FRM, CL, RSTB, ADC, CLK1, CLK2, CS1B, CS2B, CS3, E, R/W, RS and DB0~DB7.
*4. Applies V0L(R), V2L(R), V3L(R) and V5L(R).

Voltage level: VDD>V0L=VOR=V2L=V2R=V3L=V3R=V5L=V5R=VEE.
# KS0108B
## 64CH SEGMENT DRIVER FOR DOT MATRIX LCD

### ELECTRICAL CHARACTERISTICS

**DC Characteristics** ($V_{CC}=4.5-5.5V$, $V_{SS}=0V$, $V_{CC}-V_{EE}=8-17V$, $T_a=-30\sim+85^\circ C$)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input High Voltage</td>
<td>$V_{IH1}$</td>
<td>$-0.7V_{DD}$</td>
<td>2.0</td>
<td>- $V_{DD}$</td>
<td>-</td>
<td>V</td>
<td>*1</td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>$V_{IL1}$</td>
<td>0</td>
<td>- 0.3$V_{DD}$</td>
<td>-</td>
<td>V</td>
<td>*1</td>
<td></td>
</tr>
<tr>
<td>Output High Voltage</td>
<td>$V_{OH}$</td>
<td>$I_{OH}=-200\mu A$</td>
<td>2.4</td>
<td>-</td>
<td>-</td>
<td>V</td>
<td>*3</td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>$V_{OL}$</td>
<td>$I_{OL}=1.6\mu A$</td>
<td>-</td>
<td>- 0.4</td>
<td>-</td>
<td>V</td>
<td>*3</td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>$I_{LKG}$</td>
<td>$V_{IN}=V_{SS}~V_{DD}$</td>
<td>-1.0</td>
<td>-</td>
<td>1.0</td>
<td>$\mu A$</td>
<td>*4</td>
</tr>
<tr>
<td>Three-state(ON) Input Current</td>
<td>$I_{ON}$</td>
<td>$V_{IN}=V_{SS}~V_{DD}$</td>
<td>-5.0</td>
<td>-</td>
<td>5.0</td>
<td>$\mu A$</td>
<td>*5</td>
</tr>
<tr>
<td>Driver Input Leakage Current</td>
<td>$I_{DL}$</td>
<td>$V_{IN}=V_{EE}~V_{DD}$</td>
<td>-2.0</td>
<td>-</td>
<td>2.0</td>
<td>$\mu A$</td>
<td>*6</td>
</tr>
<tr>
<td>Operating Current</td>
<td>$I_{DD1}$</td>
<td>During Display</td>
<td>-</td>
<td>- 100</td>
<td>-</td>
<td>$\mu A$</td>
<td>*7</td>
</tr>
<tr>
<td></td>
<td>$I_{DD2}$</td>
<td>During Access</td>
<td>-</td>
<td>- 500</td>
<td>-</td>
<td>$\mu A$</td>
<td>*7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Access Cycle=1MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>On Resistance</td>
<td>$R_{ON}$</td>
<td>$V_{DD}-V_{EE}=15V$</td>
<td>-</td>
<td>7.5</td>
<td>-</td>
<td>K(\Omega)</td>
<td>*8</td>
</tr>
</tbody>
</table>

*1. CL, FRM, M, RSTB, CLK1, CLK2
2. CS1B, CS2B, CS3, E, R/W, RS, DB0~DB7
3. DB0~DB7
4. Excepted DB0~DB7
5. DB0~DB7 at High Impedance
6. V0L(R), V2L(R), V3L(R), V5L(R)
7. 1/84 duty, FCLK=250KHZ, Frame Frequency=70HZ, Output: No Load
8. $V_{DD}-V_{EE}=15.5V$ $V_{0L}(R)-V_{2L}(R)=V_{CC}/27$ $(V_{CC}-V_{EE})/V_{3L}(R)-V_{EE}+(27V_{CC}-V_{EE})>V_{5L}(R)$

**AC Characteristics** ($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $T_a=-30^\circ C\sim+85^\circ C$)

**Clock Timing**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK1, CLK2 Cycle Time</td>
<td>$t_{CY}$</td>
<td>2.5</td>
<td>-</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>CLK1-LOW Level Width</td>
<td>$t_{L1}$</td>
<td>625</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>CLK2-LOW Level Width</td>
<td>$t_{L2}$</td>
<td>625</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>CLK1-HIGH Level Width</td>
<td>$t_{H1}$</td>
<td>1875</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>CLK2-HIGH Level Width</td>
<td>$t_{H2}$</td>
<td>1875</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>CLK1-CLK2 Phase Difference</td>
<td>$t_{12}$</td>
<td>625</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>CLK2-CLK1 Phase Difference</td>
<td>$t_{21}$</td>
<td>625</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>CLK1, CLK2 Rise Time</td>
<td>$t_{r}$</td>
<td>-</td>
<td>-</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>CLK1, CLK2 Fall Time</td>
<td>$t_{f}$</td>
<td>-</td>
<td>-</td>
<td>150</td>
<td></td>
</tr>
</tbody>
</table>
(2) Display Control Timing

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>FRM Delay Time</td>
<td>$t_{DF}$</td>
<td>-2</td>
<td></td>
<td>+2</td>
<td>us</td>
</tr>
<tr>
<td>M Delay Time</td>
<td>$t_{DM}$</td>
<td>-2</td>
<td></td>
<td>+2</td>
<td>us</td>
</tr>
<tr>
<td>CL LOW Level Width</td>
<td>$t_{WL}$</td>
<td>35</td>
<td></td>
<td></td>
<td>us</td>
</tr>
<tr>
<td>CL HIGH Level Width</td>
<td>$t_{WH}$</td>
<td>35</td>
<td></td>
<td></td>
<td>us</td>
</tr>
</tbody>
</table>

Fig 1. External clock waveform

Fig 2. Display control signal waveform
### (3) MPU Interface

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>E Cycle</td>
<td>$t_c$</td>
<td>1000</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>E High Level Width</td>
<td>$t_{WH}$</td>
<td>450</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>E Low Level Width</td>
<td>$t_{WL}$</td>
<td>450</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>E Rise Time</td>
<td>$t_r$</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>E Fall Time</td>
<td>$t_f$</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>ns</td>
</tr>
<tr>
<td>Address Set-Up Time</td>
<td>$t_{ASU}$</td>
<td>140</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>$t_{AH}$</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Data Set-Up Time</td>
<td>$t_{DSS}$</td>
<td>200</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Data Delay Time</td>
<td>$t_{DD}$</td>
<td>-</td>
<td>-</td>
<td>320</td>
<td>ns</td>
</tr>
<tr>
<td>Data Hold Time (Write)</td>
<td>$t_{DWH}$</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Data Hold Time (Read)</td>
<td>$t_{DHR}$</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

Fig 3. MPU write timing
KS0108B  64CH SEGMENT DRIVER FOR DOT MATRIX LCD

Fig 3. MPU write timing
KS0108B 64CH SEGMENT DRIVER FOR DOT MATRIX LCD

APPLICATION CIRCUIT

1.1/64 duty common driver(KS0107B) interface circuit
KS0108B  64CH SEGMENT DRIVER FOR DOT MATRIX LCD

OPERATING PRINCIPLES & METHODS

1. I/O Buffer
   Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS1B-CS3.

2. Input register
   Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM. When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then Writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

3. Output register
   Output register stores the data temporarily from display data RAM when CS1B, CS2B, CS3 is in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H, RS=L, status data (busy check) can read out.
   To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

   RS | R/W | Function
   ---|-----|-------------------
   L  | L   | Instruction       
   H  |     | Status read (busy check)
   L  |     | Data write (from input register to display data RAM)
   H  |     | Data read (from display data RAM to output register)

4. Reset
   Reset can be initialized system by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occured.
   1. Display off
   2. Display start line register become set by 0 (Z-address 0)
   While RSTB is low, any instruction except status read can be accepted. Reset status appers at DB4. After DB4 is low, any instruction can be accepted.
   The Conditions of power supply at initial power up are shown in table 1.

Table 1. Power Supply Initial Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset Time</td>
<td>t_{RS}</td>
<td>1.0</td>
<td>-</td>
<td>-</td>
<td>us</td>
</tr>
<tr>
<td>Rise Time</td>
<td>t_{R  }</td>
<td>-</td>
<td>-</td>
<td>200</td>
<td>ns</td>
</tr>
</tbody>
</table>

The Conditions of power supply at initial power up are shown in table 1.
5. Busy flag
Busy flag indicates that KS0108B is operating or no operating. When busy flag is high, KS0108B is in internal operating. When busy flag is low, KS0108B can accept the data or instruction. DB7 indicates busy flag of the KS0108B.

6. Display On/Off Flip-Flop
The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data. The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low. The status of the flip-flop is output to DB5 by status read instruction. The display on/off flip-flop synchronized by CL signal.

7. X Page Register
X page register designates page of the internal display data RAM. It has not count function. An address is set by instruction.

8. Y address counter
Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

9. Display Data RAM
Display data RAM stores a display data for liquid crystal display. To express on state dot matrix of liquid crystal display, write data 1. The other way, off state writes 0. Display data RAM address and segment output can be controlled by ADC signal.

ADC=H, DB<0:7>=0 - Y-address 0 - A0 - S1
DB<0:7>=63 - Y-address 63 - A63 - S64
ADC=L, DB<0:7>=0 - Y-address 63 - A63 - S64
DB<0:7>=63 - A0 - S1
ADC terminal connect the VDD or VSS.

10. Display Start Line Register
The display start line register indicates of display data RAM to display top line of liquid crystal display. The display start line register is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter. It is used for scrolling of the liquid crystal display screen.
### DISPLAY CONTROL INSTRUCTION

The display control instructions control the internal state of the KS0108B. Instruction is received from MPU to KS0108B for the display control. The following table shows various instructions.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>RS</th>
<th>R/W</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Display ON/OFF</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L/H</td>
<td>Controls the display on or off. Internal status and display RAM data is not affected. L:OFF, H:ON</td>
</tr>
<tr>
<td>Set Address</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Sets the Y address in the Y address counter. (0-63)</td>
</tr>
<tr>
<td>Set Page (X address)</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td></td>
<td></td>
<td></td>
<td>Sets the X address at the X address register. (0-7)</td>
</tr>
<tr>
<td>Display Start Line</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Indicates the display data RAM displayed at the top of the screen. (0-63)</td>
</tr>
<tr>
<td>Write Display Data</td>
<td>H</td>
<td>L</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Write Data</td>
</tr>
<tr>
<td>Read Display Data</td>
<td>H</td>
<td>H</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reads data (DB0:7) from display data RAM to the data bus.</td>
</tr>
</tbody>
</table>
2. Timing diagram (1/64 duty)

CLK1

CLK2

INPUT

CL

FRM

M

COMMON

C0

C1

C2

C3

C4

C5

C6

C7

C8

C9

C10

C11

C12

C13

C14

C15

C16

C17

C18

C19

C20

C21

C22

C23

C24

C25

C26

C27

C28

C29

C30

C31

C32

C33

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C35

C36

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C43

C44

C45

C46

C47

C48

C49

C50

C51

C52

C53

C54

C55

C56

C57

C58

C59

C60

C61

C62

C63

C64

SEGMENT

S1

S2

S3

S4

S5

S6

S7

S8

S9

S10

S11

S12

S13

S14

S15

S16

S17

S18

S19

S20

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S41

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S44

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S46

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S48

S49

S50

S51

S52

S53

S54

S55

S56

S57

S58

S59

S60

S61

S62

S63

S64

\( V_0 \)

\( V_1 \)

\( V_2 \)

\( V_3 \)

\( V_4 \)

\( V_5 \)

\( V_6 \)

\( V_7 \)

\( V_8 \)

\( V_9 \)

\( V_{10} \)

\( V_{11} \)

\( V_{12} \)

\( V_{13} \)

\( V_{14} \)

\( V_{15} \)

\( V_{16} \)

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\( V_{23} \)

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\( V_{26} \)

\( V_{27} \)

\( V_{28} \)

\( V_{29} \)

\( V_{30} \)

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\( V_{32} \)

\( V_{33} \)

\( V_{34} \)

\( V_{35} \)

\( V_{36} \)

\( V_{37} \)

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\( V_{39} \)

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\( V_{41} \)

\( V_{42} \)

\( V_{43} \)

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\( V_{45} \)

\( V_{46} \)

\( V_{47} \)

\( V_{48} \)

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\( V_{50} \)

\( V_{51} \)

\( V_{52} \)

\( V_{53} \)

\( V_{54} \)

\( V_{55} \)

\( V_{56} \)

\( V_{57} \)

\( V_{58} \)

\( V_{59} \)

\( V_{60} \)

\( V_{61} \)

\( V_{62} \)

\( V_{63} \)

\( V_{64} \)

1 frame
3. LCD Panel interface application circuit

KS0108B NO. 1
S1 ... S64

KS0108B NO. 2
S1 ... S64

KS0108B NO. 8
S1 ... S64

KS0107B (Master)

C1
C2
C3
... 
C64

LCD PANEL
(128x480 dots)

KS0107B (Master)

C1
C2
C3
... 
C64

S1 ... S64
NO.3
KS0108B

S1 ... S64
NO.10
KS0108B

S1 ... S64
NO.16
KS0108B

COM1
COM2
COM3
COM64

COM5
COM6
COM7
COM128

S1 ... S64
S1 ... S64
S1 ... S64
KS0108B  64CH SEGMENT DRIVER FOR DOT MATRIX LCD

PAD DIAGRAM

CHIP SIZE : 4090μm x 4020
PAD SIZE : 100μm x 100μm
UNIT : μm

KS0108B Marking : easy to find the PAD No.30
## PAD LOCATION

<table>
<thead>
<tr>
<th>PAD NUMBER</th>
<th>PAD NAME</th>
<th>COORDINATE X</th>
<th>COORDINATE Y</th>
<th>PAD NUMBER</th>
<th>COORDINATE X</th>
<th>COORDINATE Y</th>
<th>PAD NUMBER</th>
<th>COORDINATE X</th>
<th>COORDINATE Y</th>
<th>PAD NUMBER</th>
<th>COORDINATE X</th>
<th>COORDINATE Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ADC</td>
<td>-1140</td>
<td>1845</td>
<td>35</td>
<td>S38</td>
<td>-687</td>
<td>-1845</td>
<td>69</td>
<td>S4</td>
<td>1882</td>
<td>791</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>M</td>
<td>-1225</td>
<td>1845</td>
<td>36</td>
<td>S37</td>
<td>-562</td>
<td>-1845</td>
<td>70</td>
<td>S3</td>
<td>1882</td>
<td>916</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>VDD</td>
<td>-1410</td>
<td>1845</td>
<td>37</td>
<td>S36</td>
<td>-437</td>
<td>-1845</td>
<td>71</td>
<td>S2</td>
<td>1882</td>
<td>1041</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>V3H</td>
<td>-1882</td>
<td>1805</td>
<td>38</td>
<td>S35</td>
<td>-312</td>
<td>-1845</td>
<td>72</td>
<td>S1</td>
<td>1882</td>
<td>1166</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>V2R</td>
<td>-1882</td>
<td>1884</td>
<td>39</td>
<td>S34</td>
<td>-197</td>
<td>-1845</td>
<td>73</td>
<td>VEE1</td>
<td>1882</td>
<td>1210</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>VSR</td>
<td>-1882</td>
<td>1858</td>
<td>40</td>
<td>S33</td>
<td>-62</td>
<td>-1845</td>
<td>74</td>
<td>VOL</td>
<td>1882</td>
<td>1385</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>VOR</td>
<td>-1882</td>
<td>1434</td>
<td>41</td>
<td>S32</td>
<td>62</td>
<td>-1845</td>
<td>75</td>
<td>V0L</td>
<td>1882</td>
<td>1559</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>VEE2</td>
<td>-1882</td>
<td>1309</td>
<td>42</td>
<td>S31</td>
<td>187</td>
<td>-1845</td>
<td>76</td>
<td>V2L</td>
<td>1882</td>
<td>1684</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>S64</td>
<td>-1882</td>
<td>1165</td>
<td>43</td>
<td>S30</td>
<td>312</td>
<td>-1845</td>
<td>77</td>
<td>V3L</td>
<td>1882</td>
<td>1809</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>S63</td>
<td>-1882</td>
<td>1040</td>
<td>44</td>
<td>S29</td>
<td>437</td>
<td>-1845</td>
<td>78</td>
<td>VSS</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>S62</td>
<td>-1882</td>
<td>915</td>
<td>45</td>
<td>S28</td>
<td>562</td>
<td>-1845</td>
<td>79</td>
<td>DB0</td>
<td>1277</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>S61</td>
<td>-1882</td>
<td>790</td>
<td>46</td>
<td>S27</td>
<td>687</td>
<td>-1845</td>
<td>80</td>
<td>DB1</td>
<td>1142</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>S60</td>
<td>-1882</td>
<td>665</td>
<td>47</td>
<td>S26</td>
<td>812</td>
<td>-1845</td>
<td>81</td>
<td>DB2</td>
<td>1007</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>S59</td>
<td>-1882</td>
<td>540</td>
<td>48</td>
<td>S25</td>
<td>937</td>
<td>-1845</td>
<td>82</td>
<td>DB3</td>
<td>882</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>S58</td>
<td>-1882</td>
<td>419</td>
<td>49</td>
<td>S24</td>
<td>1062</td>
<td>-1845</td>
<td>83</td>
<td>DB4</td>
<td>751</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>S57</td>
<td>-1882</td>
<td>290</td>
<td>50</td>
<td>S23</td>
<td>1187</td>
<td>-1845</td>
<td>84</td>
<td>DB5</td>
<td>632</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>S56</td>
<td>-1882</td>
<td>166</td>
<td>51</td>
<td>S22</td>
<td>1487</td>
<td>-1845</td>
<td>85</td>
<td>DB6</td>
<td>507</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>S55</td>
<td>-1882</td>
<td>40</td>
<td>52</td>
<td>S21</td>
<td>1882</td>
<td>-1379</td>
<td>86</td>
<td>DB7</td>
<td>382</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>S54</td>
<td>-1882</td>
<td>-84</td>
<td>53</td>
<td>S20</td>
<td>1882</td>
<td>-1239</td>
<td>87</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>S53</td>
<td>-1882</td>
<td>-209</td>
<td>54</td>
<td>S19</td>
<td>1882</td>
<td>-1099</td>
<td>88</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>S52</td>
<td>-1882</td>
<td>-334</td>
<td>55</td>
<td>S18</td>
<td>1882</td>
<td>-959</td>
<td>89</td>
<td>NC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>S51</td>
<td>-1882</td>
<td>-459</td>
<td>56</td>
<td>S17</td>
<td>1882</td>
<td>-834</td>
<td>90</td>
<td>CS3</td>
<td>245</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>S50</td>
<td>-1882</td>
<td>-584</td>
<td>57</td>
<td>S16</td>
<td>1882</td>
<td>-709</td>
<td>91</td>
<td>CS2B</td>
<td>120</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>S49</td>
<td>-1882</td>
<td>-709</td>
<td>58</td>
<td>S15</td>
<td>1882</td>
<td>-584</td>
<td>92</td>
<td>CS1B</td>
<td>5</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>S48</td>
<td>-1882</td>
<td>-834</td>
<td>59</td>
<td>S14</td>
<td>1882</td>
<td>-459</td>
<td>93</td>
<td>DB7</td>
<td>130</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>S47</td>
<td>-1882</td>
<td>-959</td>
<td>60</td>
<td>S13</td>
<td>1882</td>
<td>-394</td>
<td>94</td>
<td>R.W</td>
<td>365</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>S46</td>
<td>-1882</td>
<td>-1089</td>
<td>61</td>
<td>S12</td>
<td>1882</td>
<td>-209</td>
<td>95</td>
<td>RS</td>
<td>-380</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>S45</td>
<td>-1882</td>
<td>-1239</td>
<td>62</td>
<td>S11</td>
<td>1882</td>
<td>-84</td>
<td>96</td>
<td>CL</td>
<td>-505</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>S44</td>
<td>-1882</td>
<td>-1379</td>
<td>63</td>
<td>S10</td>
<td>1882</td>
<td>41</td>
<td>97</td>
<td>CLK2</td>
<td>630</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>S43</td>
<td>-1882</td>
<td>-1845</td>
<td>64</td>
<td>S9</td>
<td>1882</td>
<td>166</td>
<td>98</td>
<td>CLK1</td>
<td>-755</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>S42</td>
<td>-1187</td>
<td>-1845</td>
<td>65</td>
<td>S8</td>
<td>1882</td>
<td>291</td>
<td>99</td>
<td>E</td>
<td>-880</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>S41</td>
<td>-1062</td>
<td>-1845</td>
<td>66</td>
<td>S7</td>
<td>1882</td>
<td>416</td>
<td>100</td>
<td>FRM</td>
<td>-1005</td>
<td>1845</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>S40</td>
<td>-937</td>
<td>-1845</td>
<td>67</td>
<td>S6</td>
<td>1882</td>
<td>541</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>S39</td>
<td>-812</td>
<td>-1845</td>
<td>68</td>
<td>S5</td>
<td>1882</td>
<td>666</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>