

AZ DISPLAYS, INC.

COMPLETE LCD SOLUTIONS

SPECIFICATIONS FOR LIQUID CRYSTAL DISPLAY

PART NUMBER:

AGM1264P SERIES

DATE:

August 17, 2006

AGM1264P SERIES LCD MODULE

GENERAL SPECIFICATION

Interface With Parallel MPU

Driving IC:S1D15605

Display Specification

Display Dot Matrix :128*64

Viewing Angle :6:00 Clock

Display Duty:1/65 Driving bias:1/9 Driving voltage:8.9V

Mechanical Characteristics(Unit:mm)

Extenal Dimension:89.7*49.8*6.0

View Area:66.8*35.5

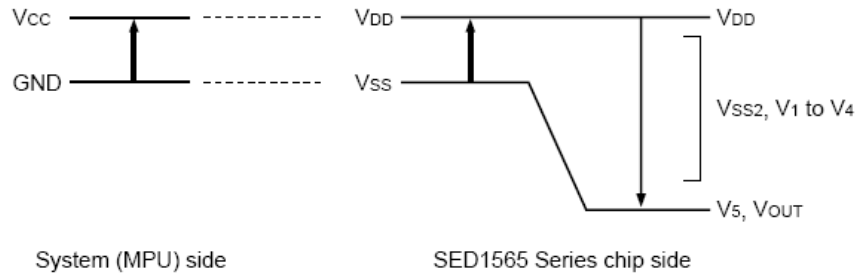
Dots Size:0.48*0.48

Dots Pitch:0.50*0.50

AGM1264P SERIES LCD MODULE

Absolute Maximun Ratings

| Parameter | | Symbol | Conditions | Unit |
|--|--|----------------|-------------------|------|
| Power Supply Voltage | | VDD | -0.3 to +7.0 | V |
| Power supply voltage (2) (VDD standard) | With Triple step-up With Quad step-up | VSS2 | -7.0 to +0.3 | V |
| | | | -6.0 to +0.3 | |
| | | | -4.5 to +0.3 | |
| Power supply voltage (3) (VDD standard) | | V5, VOUT | -18.0 to +0.3 | V |
| Power supply voltage (4) (VDD standard) | | V1, V2, V3, V4 | V5 to +0.3 | V |
| Input voltage | | VIN | -0.3 to VDD + 0.3 | V |
| Output voltage | | VO | -0.3 to VDD + 0.3 | V |
| Operating temperature | | TOPR | -40 to +85 | °C |
| Storage temperature | TCP | TSTR | -55 to +100 | °C |
| | Bare chip | | -55 to +125 | |



Notes and Cautions

1. The VSS2, V1 to V5 and VOUT are relative to the VDD = 0V reference.
2. Insure that the voltage levels of V1, V2, V3, and V4 are always such that $VDD \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

Electrical Characteristics

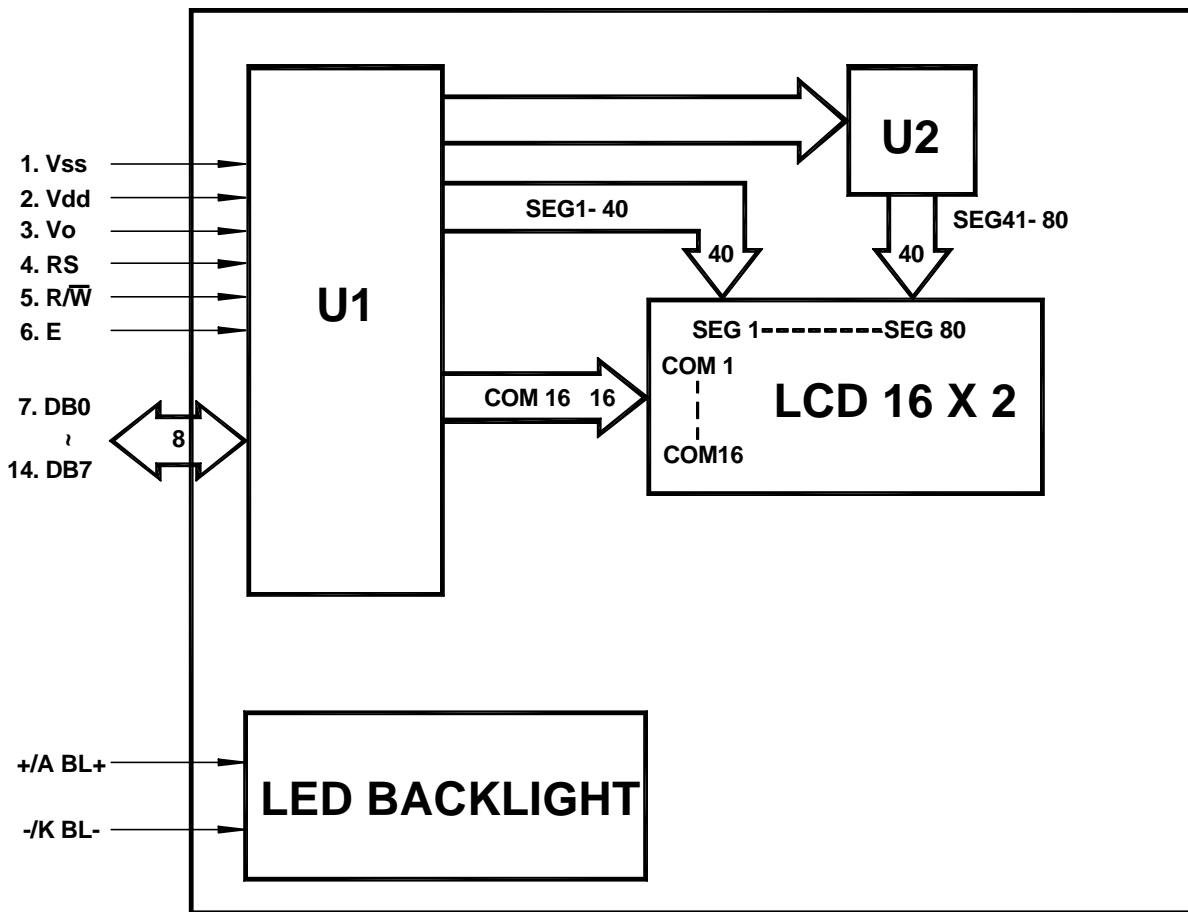
| Item | Symbol | Condition | Standard Value | | | Unit |
|--------------------------|---------|-----------|----------------|------|--------|------|
| | | | Min | Type | Max | |
| Supply Voltage For logic | Vdd-Vss | - | 1.8 | - | 5.5 | V |
| Supply Current For logic | Idd | - | - | - | 1000 | uA |
| Driving Current For LCD | Iee | | - | - | 80 | uA |
| Driving Voltage For LCD | V0-Vss | | - | - | - | V |
| Input Voltage H level | Vih | | 0.7Vdd | - | Vdd | V |
| Input Voltage L level | Vil | | Vss | - | 0.3Vdd | V |

AGM1264P SERIES LCD MODULE

4.1 OPTICAL CHARACTERISTICS (Ta=25°C, Vdd= 5.0V±0.25V, STN LC fluid)

| Item | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------------|----------|--------------------------------|-----|-----|-----|------|
| Viewing angle (horizontal) | θ | $Cr \geq 2.0$ | -60 | - | 35 | deg |
| Viewing angle (vertical) | ϕ | $Cr \geq 2.0$ | -40 | - | 40 | deg |
| Contrast Ratio | Cr | $\phi=0^\circ, \theta=0^\circ$ | - | 6 | - | |
| Response time (rise) | Tr | $\phi=0^\circ, \theta=0^\circ$ | - | 150 | 250 | ms |
| Response time (fall) | Tf | $\phi=0^\circ, \theta=0^\circ$ | - | 150 | 250 | ms |

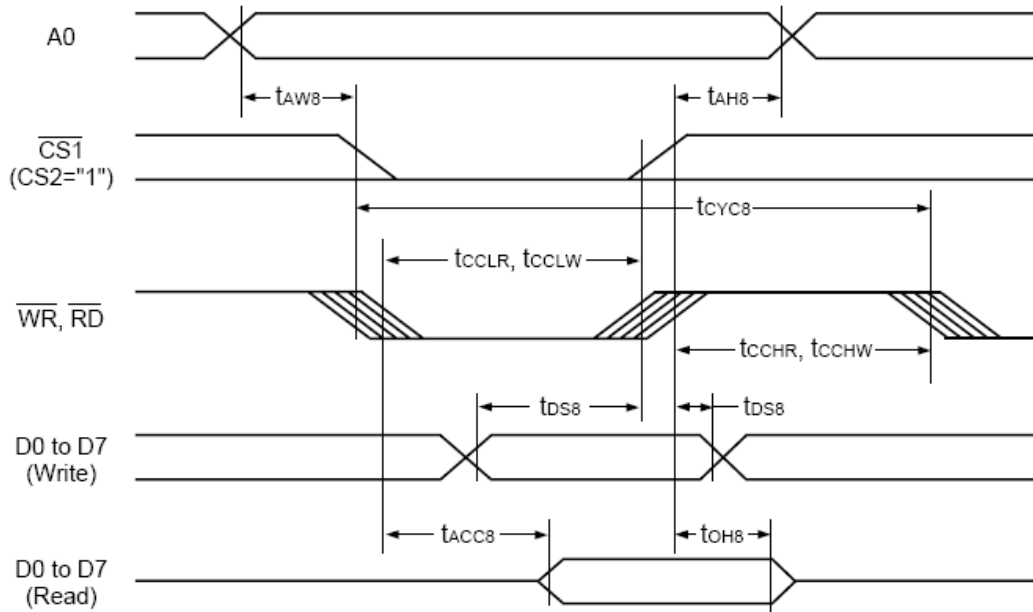
5.0 BLOCK DIAGRAM



AGM1264P SERIES LCD MODULE

TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)



(VDD = 4.5 V to 5.5 V, Ta = -40 to 85°C)

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|-----------------|--------|-------------|--------|-----|-------|
| | | | | Min | Max | |
| Address hold time | A0 | tAH8 | | 0 | — | ns |
| Address setup time | A0 | tAW8 | | 0 | — | ns |
| System cycle time | A0 | tCYC8 | | 166 | — | ns |
| Control L pulse width (\overline{WR}) | \overline{WR} | tcCLW | | 30 | — | ns |
| Control L pulse width (\overline{RD}) | \overline{RD} | tcCLR | | 70 | — | ns |
| Control H pulse width (\overline{WR}) | \overline{WR} | tcCHW | | 30 | — | ns |
| Control H pulse width (\overline{RD}) | \overline{RD} | tcCHR | | 30 | — | ns |
| Data setup time | D0 to D7 | tDS8 | | 30 | — | ns |
| Address hold time | | tDH8 | | 10 | — | ns |
| \overline{RD} access time | | tACC8 | CL = 100 pF | — | 70 | ns |
| Output disable time | | toH8 | | 5 | 50 | ns |

(VDD = 2.7 V to 4.5 V, Ta = -40 to 85°C)

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|-----------------|--------|-------------|--------|-----|-------|
| | | | | Min | Max | |
| Address hold time | A0 | tAH8 | | 0 | — | ns |
| Address setup time | A0 | tAW8 | | 0 | — | ns |
| System cycle time | A0 | tCYC8 | | 300 | — | ns |
| Control L pulse width (\overline{WR}) | \overline{WR} | tcCLW | | 60 | — | ns |
| Control L pulse width (\overline{RD}) | \overline{RD} | tcCLR | | 120 | — | ns |
| Control H pulse width (\overline{WR}) | \overline{WR} | tcCHW | | 60 | — | ns |
| Control H pulse width (\overline{RD}) | \overline{RD} | tcCHR | | 60 | — | ns |
| Data setup time | D0 to D7 | tDS8 | | 40 | — | ns |
| Address hold time | | tDH8 | | 15 | — | ns |
| \overline{RD} access time | | tACC8 | CL = 100 pF | — | 140 | ns |
| Output disable time | | toH8 | | 10 | 100 | ns |

AGM1264P SERIES LCD MODULE

(VDD = 1.8 V to 2.7 V, Ta = -40 to 85°C)

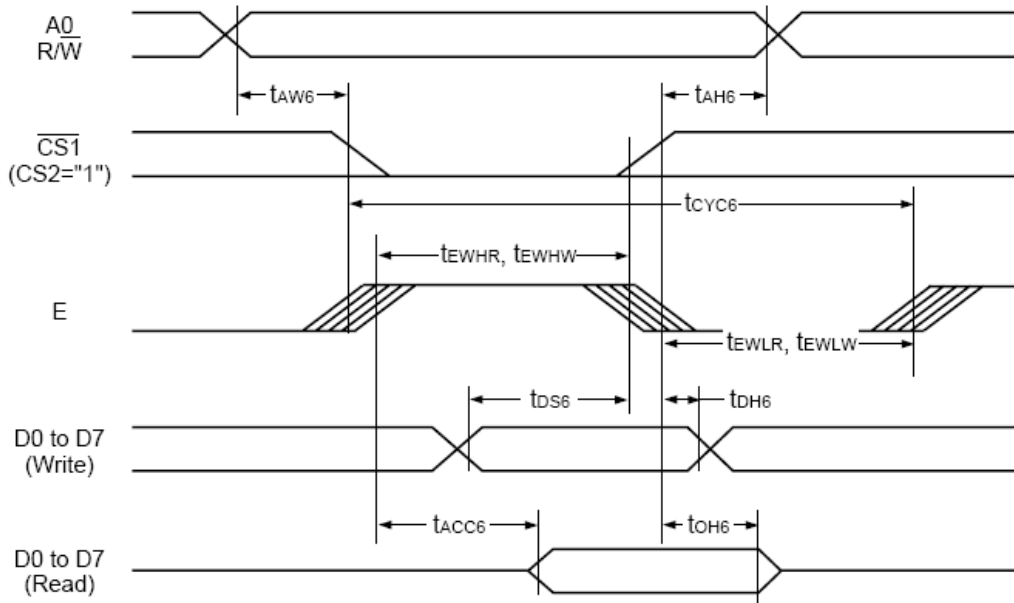
| Item | Signal | Symbol | Condition | Rating | | Units |
|---|-----------------|-------------------|-------------|--------|-----|-------|
| | | | | Min | Max | |
| Address hold time | A0 | t _{AH8} | | 0 | — | ns |
| Address setup time | A0 | t _{AW8} | | 0 | — | ns |
| System cycle time | A0 | t _{CYC8} | | 1000 | — | ns |
| Control L pulse width (\overline{WR}) | \overline{WR} | t _{CCLW} | | 120 | — | ns |
| Control L pulse width (\overline{RD}) | \overline{RD} | t _{CCLR} | | 240 | — | ns |
| Control H pulse width (\overline{WR}) | \overline{WR} | t _{CCHW} | | 120 | — | ns |
| Control H pulse width (\overline{RD}) | \overline{RD} | t _{CCHR} | | 120 | — | ns |
| Data setup time | D0 to D7 | t _{DS8} | | 80 | — | ns |
| Address hold time | | t _{DH8} | | 30 | — | ns |
| \overline{RD} access time | | t _{ACC8} | CL = 100 pF | — | 280 | ns |
| Output disable time | | t _{OH8} | | 10 | 200 | ns |

*1 The input signal rise time and fall time (tr, tr) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tr) ≤ (tcyc8 - tcclw - tcchwh) for (tr + tr) ≤ (tcyc8 - tcclr - tcchr) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

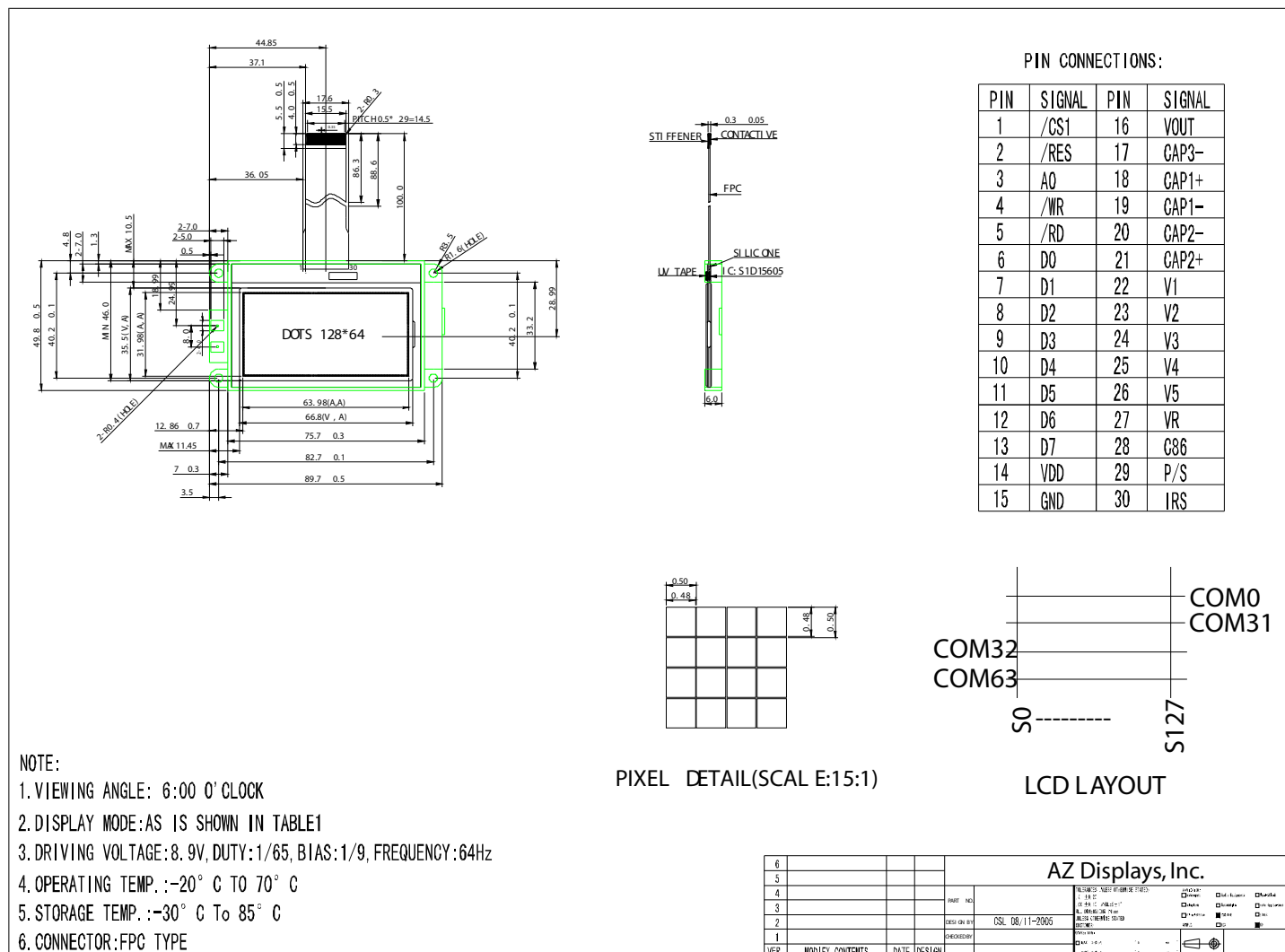
*3 tcclw and tcclr are specified as the overlap between CS1 being "L" (CS2 = "H") and \overline{WR} and \overline{RD} being at the "L" level.

System Bus Read/Write Characteristics 2 (6800 Series MPU)



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9.0 MECHANICAL DIAGRAM



AGM1264P SERIES LCD MODULE

(VDD = 4.5 V to 5.5 V, Ta = -40 to 85°C)

| Item | Signal | Symbol | Condition | Rating | | Units | |
|---------------------|---------------|--------|-----------|-------------|-----|-------|----|
| | | | | Min | Max | | |
| Address hold time | A0 | tAH6 | | 0 | — | ns | |
| Address setup time | | tAW6 | | 0 | — | ns | |
| System cycle time | A0 | tCYC6 | | 166 | — | ns | |
| Data setup time | D0 to D7 | tDS6 | | 30 | — | ns | |
| Data hold time | | tDH6 | | 10 | — | ns | |
| Access time | | tACC6 | | CL = 100 pF | — | 70 | ns |
| Output disable time | | tOH6 | | | 10 | 50 | ns |
| Enable H pulse time | Read Write | E | | tEWHR | 70 | — | ns |
| | | | | tEWHW | 30 | — | ns |
| Enable L pulse time | Read Write | E | | tEWLR | 30 | — | ns |
| | | | | tEWLW | 30 | — | ns |

(VDD = 2.7 V to 4.5 V, Ta = -40 to 85°C)

| Item | Signal | Symbol | Condition | Rating | | Units | |
|---------------------|---------------|--------|-----------|-------------|-----|-------|----|
| | | | | Min | Max | | |
| Address hold time | A0 | tAH6 | | 0 | — | ns | |
| Address setup time | | tAW6 | | 0 | — | ns | |
| System cycle time | A0 | tCYC6 | | 300 | — | ns | |
| Data setup time | D0 to D7 | tDS6 | | 40 | — | ns | |
| Data hold time | | tDH6 | | 15 | — | ns | |
| Access time | | tACC6 | | CL = 100 pF | — | 140 | ns |
| Output disable time | | tOH6 | | | 10 | 100 | ns |
| Enable H pulse time | Read Write | E | | tEWHR | 120 | — | ns |
| | | | | tEWHW | 60 | — | ns |
| Enable L pulse time | Read Write | E | | tEWLR | 60 | — | ns |
| | | | | tEWLW | 60 | — | ns |

(VDD = 1.8 V to 2.7 V, Ta = -40 to 85°C)

| Item | Signal | Symbol | Condition | Rating | | Units | |
|---------------------|---------------|--------|-----------|-------------|-----|-------|----|
| | | | | Min | Max | | |
| Address hold time | A0 | tAH6 | | 0 | — | ns | |
| Address setup time | | tAW6 | | 0 | — | ns | |
| System cycle time | A0 | tCYC6 | | 1000 | — | ns | |
| Data setup time | D0 to D7 | tDS6 | | 80 | — | ns | |
| Data hold time | | tDH6 | | 30 | — | ns | |
| Access time | | tACC6 | | CL = 100 pF | — | 280 | ns |
| Output disable time | | tOH6 | | | 10 | 200 | ns |
| Enable H pulse time | Read Write | E | | tEWHR | 240 | — | ns |
| | | | | tEWHW | 120 | — | ns |
| Enable L pulse time | Read Write | E | | tEWLR | 120 | — | ns |
| | | | | tEWLW | 120 | — | ns |

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC6 - tEWLW - tEWHW) for (tr + tf) ≤ (tCYC6 - tEWLR - tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CS1 being "L" (CS2 = "H") and E.

IC Specification

See The Reference of EPSON Data Book----S1D15605

AGM1264P SERIES LCD MODULE

Instruction Table

| Command | Command Code | | | | | | | | | | | Function | |
|---|--------------|-----------------|-----------------|------------|----|-------------------------|----|----------------------------------|----------------|----|------|----------|--|
| | A0 | \overline{RD} | \overline{WR} | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| (1) Display ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 1 | LCD display ON/OFF 0: OFF, 1: ON |
| (2) Display start line set | 0 | 1 | 0 | 0 | 1 | Display start address | | | | | | 0 | Sets the display RAM display start line address |
| (3) Page address set | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Page address | | | | 0 | Sets the display RAM page address |
| (4) Column address set upper bit | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Most significant column address | | | | 0 | Sets the most significant 4 bits of the display RAM column address. |
| Column address set lower bit | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Least significant column address | | | | 0 | Sets the least significant 4 bits of the display RAM column address. |
| (5) Status read | 0 | 0 | 1 | Status | | | | 0 | 0 | 0 | 0 | 0 | Reads the status data |
| (6) Display data write | 1 | 1 | 0 | Write data | | | | | | | | 0 | Writes to the display RAM |
| (7) Display data read | 1 | 0 | 1 | Read data | | | | | | | | 0 | Reads from the display RAM |
| (8) ADC select | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 1 | Sets the display RAM address SEG output correspondence 0: normal, 1: reverse |
| (9) Display normal/reverse | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 1 | Sets the LCD display normal/reverse 0: normal, 1: reverse |
| (10) Display all points ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 1 | Display all points 0: normal display 1: all points ON |
| (11) LCD bias set | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 1 | Sets the LCD drive voltage bias ratio SED1565*** 0: 1/9, 1: 1/7 SED1566*** /SED1568*** /SED1569*** 0: 1/8, 1: 1/6 SED1567*** 0: 1/6, 1: 1/5 |
| (12) Read/modify/write | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Column address increment At write: +1 At read: 0 |
| (13) End | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Clear read/modify/write |
| (14) Reset | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Internal reset |
| (15) Common output mode select | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | * | * | * | 1 | Select COM output scan direction 0: normal direction, 1: reverse direction |
| (16) Power control set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Operating mode | | | 0 | Select internal power supply operating mode |
| (17) Vs voltage regulator internal resistor ratio set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Resistor ratio | | | 0 | Select internal resistor ratio (Rb/Ra) mode |
| (18) Electronic volume mode set | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Set the Vs output voltage electronic volume register |
| Electronic volume register set | 0 | 1 | 0 | * | * | Electronic volume value | | | | | | 0 | |
| (19) Static indicator ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 1 | 0: OFF, 1: ON |
| Static indicator register set | 0 | 1 | 0 | * | * | * | * | * | * | * | Mode | 0 | Set the flashing mode |
| (20) Power saver | | | | | | | | | | | | | Display OFF and display all points ON compound command |
| (21) NOP | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | Command for non-operation |
| (22) Test | 0 | 1 | 0 | 1 | 1 | 1 | 1 | * | * | * | * | * | Command for IC test. Do not use this command |

(Note) *: disabled data

AGM1264P SERIES LCD MODULE

Instruction Description

1. Display On/Off

| | | | | | | | | | | |
|----|---|----|----|----|----|----|----|----|----|-----------|
| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | - |

D0=1 Display On

D0=0 Display Off

2. Set Display Start Line

| | | | | | | | | | | |
|----|---|----|----|----|------------|------------|------------|------------|------------|------------|
| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 1 | ST5 | ST4 | ST3 | ST2 | ST1 | ST0 |

| ST5 | ST4 | ST3 | ST2 | ST1 | ST0 | Line Address |
|------------|------------|------------|------------|------------|------------|--------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| . | . | . | . | . | . | . |
| 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

3. Set Page Address

| | | | | | | | | | | |
|----|---|----|----|----|----|----|-----------|-----------|-----------|-----------|
| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | P3 | P2 | P1 | P0 |

| P3 | P2 | P1 | P0 | Page |
|-----------|-----------|-----------|-----------|------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| . | . | . | . | . |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |

4. Set Column Address

| | | | | | | | | | | |
|----|---|----|----|----|----|----|-----------|-----------|-----------|-----------|
| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | Y7 | Y6 | Y5 | Y4 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | Y3 | Y2 | Y1 | Y0 |

Y4-Y7 :Higter Bits

Y0-Y3 :Lower Bits

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| Y7 | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 | Column Address |
|----|----|----|----|----|----|----|----|----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| . | . | . | . | . | . | . | . | . |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 130 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 131 |

5. Read Status

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|--------|----|----|----|----|----|----|----|
| 0 | 0 | 1 | Status | | | | 0 | 0 | 0 | 0 |

6. Write Display Data

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|------------|----|----|----|----|----|----|----|
| 1 | 1 | 0 | Write Data | | | | | | | |

7. Read Display Data

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|-----------|----|----|----|----|----|----|----|
| 1 | 0 | 1 | Read Data | | | | | | | |

8. ADC Select

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | - |

D0=1 Display Reverse

D0=0 Display Normal

9. Normal/Reverse Display

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D |

When **D**=1 Reverse Display

D=0 Normal Display

10. Entire Display On/Off

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | D |

When D=0 Normal Display D=1 Reverse Display

11. Set LCD Bias

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | D |

When **D**=0 Bias=1/9

D=1 Bias=1/7

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Read-Modify-Write

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

13. End

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

14. Reset

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

15. Command Output Mode Select

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|-----------|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | D | * | * | * |

16. Set Power Control

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|-----------|-----------|-----------|
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | A2 | A1 | A0 |

When **A0**=1 Follower Circuit Is Turn On

A1=1 Regulator Circuit Is Turn On

A2=1 Booster Circuit Is Turn On

17. V0 Voltage Regulator Internal Resistor Ratio Set

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | R2 | R1 | R0 |

18. The Electronic Volume Mode Set

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

19. Electronic Volume Register Set

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|------------|------------|------------|------------|------------|------------|
| 0 | 1 | 0 | 0 | 0 | SV5 | SV4 | SV3 | SV2 | SV1 | SV0 |

20. Static Indicator On/Off

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|-----------|
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | D |

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21.Nop

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

22.Booster Ratio Select Mode Set

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

23.Booster Ratio Register Set

| A0 | E | RW | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|---|----|----|----|----|----|----|----|----|----|
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

D1、D0=00,2x,3x,4x

D1、D0=01,5x

D1、D0=11,6x

Application Example

Application Circuit

